

Sequential Logic Design

ONE MARK QUESTIONS

- 8.1 Writing equations for D_1 , D_2 inputs and state table for the counter.

$$\therefore D_1 = \overline{Q_1} \overline{Q_2} \text{ and } D_2 = Q_1.$$

Assuming initially output of both flip-flops is zero.

It is clear from the state table that there are only 3 states in this counter.

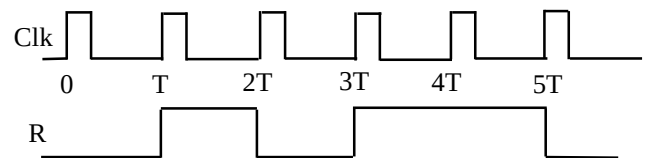
So, the output frequency = $12 \text{ kHz}/3 = 4 \text{ kHz}$.

- 8.2 There are 5 inverters in chain. So, total propagation delay = $100 \text{ pS} \times 5 = 500 \text{ pS}$. This means clock will be ON for 500 pS and OFF for 500 pS . Therefore, the periodicity of oscillator output = 1000 pS . Hence, fundamental frequency of oscillator = 1 GHz which is option 'c'.

Q_1	Q_2	D_1	D_2	Q_1^+	Q_2^+	State
0	0	1	0	1	0	S0
1	0	0	1	0	1	S1
0	1	0	0	0	0	S2
0	0	1	0	1	0	S0

- 8.3 It is clear from the diagram that it is a circular shift register. Writing state table for the output.

Clk	Q_1	Q_2	Q_3	Q_4	Q_5	$R = Q_3 + Q_5$
0	0	1	0	1	0	0
1	0	0	1	0	1	1
2	1	0	0	1	0	0
3	0	1	0	0	1	1
4	1	0	1	0	0	1
5	0	1	0	1	0	0



Drawing waveforms from the truth table, as shown in figure, we can calculate average power across resistor. We know that average power

$$P_{avg} = \frac{1}{T} \int_0^T \frac{V_t^2}{R} dt$$

$$\therefore P_{avg} = \frac{1}{5T} \left(\int_0^T 0 dt + \int_T^{2T} \frac{25}{10} dt + \int_{2T}^{3T} 0 dt + \int_{3T}^{5T} \frac{25}{10} dt \right) mW$$

$$\therefore P_{avg} = \frac{1}{5} \left(0 + \frac{25}{10} + 0 + \frac{25}{10} \times 2 \right) mW = 1.5 mW$$

- 8.4 The output of XNOR gate is low whenever odd number of inputs are high. This condition will occur when count value = 4 and the counter will reset because clear signal is active low. We know that MOD value = count + 1. So, it is a MOD 5 counter and option 'c' is correct.
- 8.5 Output Q of both flip-flops must be 1 to obtain $Y = 1$. It is possible when initial output $\bar{Q}$ of the first flip-flop is high (i.e. $Q = 0$) and in the subsequent state output Q shall change to 1 (i.e. $\bar{Q} = 0$). This entails that the Data input must be changed from '0' to '1.' So, the correct option is 'a'.
- 8.6 The counter counts from 0 to 6. So, it is a UP counter. After 6, in the next state, count value will become 7 which is undesired and counter must be reset immediately. Therefore, bit pattern 111 has to be decoded

to generate a reset pulse and 3 input AND gate can be built using two AND gates. So, the correct option is 'd'.

TWO MARKS QUESTIONS

8.1 Writing equations for D_A , D_B inputs and state table for the given finite state machine.

$$D_A = Q_A \oplus Q_B \quad \text{and} \quad D_B = \overline{Q_A X_{IN}}$$

From the state table it is clear that when $X_{IN} = 0$, FSM cycles through only 2 states whereas, $X_{IN} = 1$, FSM cycles through all of the four possible states. Hence, both options 'a' and 'd' are correct.

X_{IN}	Q_A	Q_B	D_A	D_B	Q_A^+	Q_B^+	State
0	0	0	0	1	0	1	S_1
0	0	1	1	1	1	1	S_3
0	1	0	1	1	1	1	S_3
0	1	1	0	1	0	1	S_1
1	0	0	0	1	0	1	S_1
1	0	1	1	1	1	1	S_3
1	1	0	1	0	1	0	S_2
1	1	1	0	0	0	0	S_0

8.2 Writing state table for the given finite state machine.

A	B	C	D	$D_{in} = A \oplus D$	# of clk
1	1	0	1	0	0
0	1	1	0	0	1
0	0	1	1	1	2
1	0	0	1	0	3
0	1	0	0	0	4
0	0	1	0	0	5
0	0	0	1	1	6
1	0	0	0	1	7
1	1	0	0	1	8
1	1	1	0	1	9
1	1	1	1	0	10

It is clear from this Table that after 10 clock cycles desired pattern is produced at the output.

8.3 The counter is synchronous counter and the decoding gate will be active when count = 110. But the decoding gate delay (2 nS) is more than the clock pulse duration (1nS). Hence, count will increment before reset pulse is being applied as a result final count value will reach to 111. Therefore, it is a Mod 8 counter and option 'd' is correct.

8.4 Writing state table for the given finite state machine.

Q_1	Q_2	$J_1 = \overline{Q_2}$	$K_1 = Q_2$	$J_2 = Q_1$	$K_2 = \overline{Q_1}$
0	0	1	0	0	1
1	0	1	0	1	0
1	1	0	1	1	0
0	1	0	1	0	1
0	0	1	0	0	1

It is clear from this table that the sequence generated at Q_1 upon application of clock signal is 01100 which is given in option 'd'.

8.5 Writing state table for the given synchronous counter.

PS		NS			
Q_B	Q_A	Q_B^+	Q_A^+	D_B	D_A
0	0	1	1	1	1
1	1	0	1	0	1
0	1	1	0	1	0
1	0	0	0	0	0

It is clear from this table that

$$D_A = (Q_A Q_B + \overline{Q_A} \overline{Q_B}), D_B = Q_B$$

So, option 'd' is correct.

- 8.6** It is understood from the figure that it is an asynchronous counter. Since J and K inputs of both flip-flops are connected to logic-1, they will toggle on the rising edge of the clock signal. As there are two flip-flops the period of final output is $Clk/4$ and considering propagation delay of each flip-flop the clock edge will get shifted by $2(\Delta T)$. So, option 'c' will be correct.